ABSTRACT

A PLL circuit and an information reproduction apparatus able to reduce an influence of erroneous detection even when erroneous detection of a frequency comparator occurs and able to realize stable and high speed frequency lock-in, having a frequency comparator 25 fetching a zero cross signal ZC in synchronization with clocks CLKA to CLKC from a VCO 23 and observing from which phase to which phase an edge of the zero cross changed in synchronization with the clock CLKA and thereby detecting high/low of the frequency as frequency error and outputting an up signal UP or a down signal DOWN, an integration circuit 26 integrating the signal UP or DOWN, a comparator 27 receiving the integrated up signal UP or down signal DOWN, judging a direction of the frequency error, and outputting three signals of UPM, DOWNM, and NONM, and a gain adjustment circuit 28 determining whether or not the signal is to be output or determining a feedback gain from the pattern of a sequence of the signals UPM, DOWNM, and NONM, and outputting the same.